Signal Integrity: Faster and Simpler Debugging with Integrated Digital and Analog Measurement

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▶ Four steps to debugging signal integrity problems in high-speed digital systems.

What is Signal Integrity? Signal Integrity engineering is an activity performed during the design phase of a digital system to assure that it fully meets specifications. Signal Integrity encompasses design issues such as maximizing timing and noise margins and understanding analog characteristics such as waveforms, crosstalk, and Electro-Magnetic Interference. These second and third order effects become first order as system performance rises. Controlling them can mean the difference between project success and failure.

In the past, there was a distinct difference between digital designs and analog designs. Digital designers were not concerned with analog signal integrity because the data signals and clocks in the systems they were designing were only operating in the 10's of megahertz range. This has not been the case since CMOS and Bi-CMOS devices with sub-nanosecond rise-times have replaced slower devices. Digital designers must now be able to see both digital and analog signal characteristics to effectively debug and verify their systems.

Step #1 - The Symptom

Often during the hardware-software integration process, a digital system exhibits erratic operation when it is brought up to full clock speed. The hardware and software teams have independently developed and verified their parts of the system but when these two are integrated, the system intermittently malfunctions. Because "everything checked out" earlier, this can be a frustrating and time-consuming problem to debug. The symptom is generally obvious; the system isn't functioning properly. Finding the cause of the mal-function is the real challenge.

Step #2 - The Cause of the symptom

It's a matter of speed — edge speed that is. CMOS and Bi-CMOS devices are designed to operate in the 100's of megahertz range. Even when these devices are used in systems operating at lower frequencies, their 'digital' signals have fast rise and fall times.

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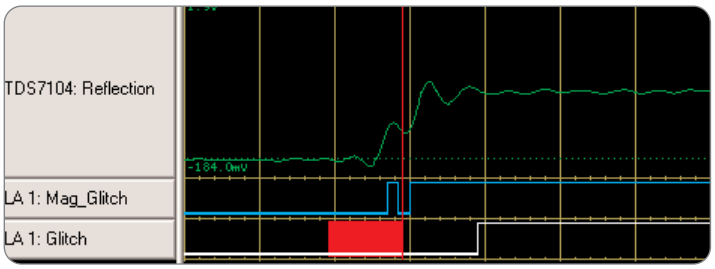
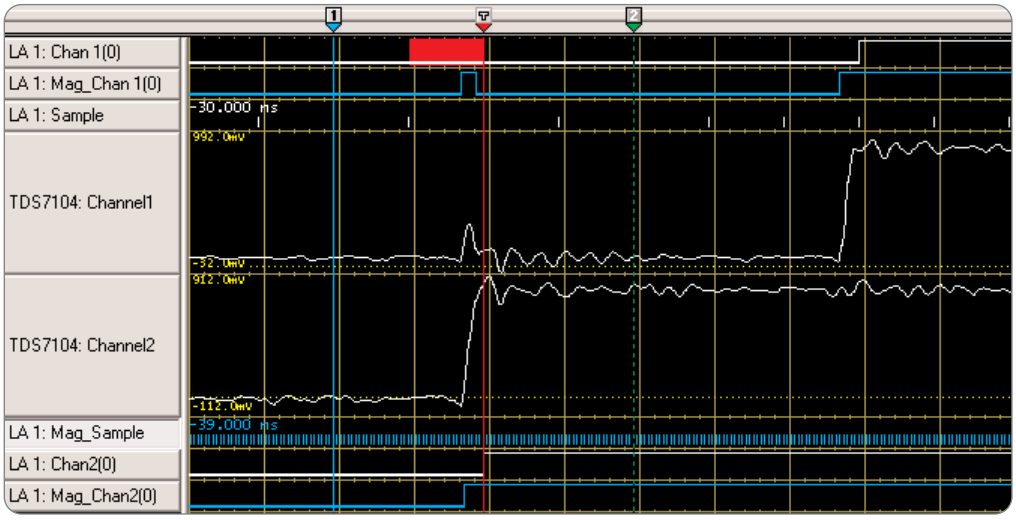


▶ ***Figure 1.*** *The reflection (step) on the rising edge is the result of improper circuit board run termination.*

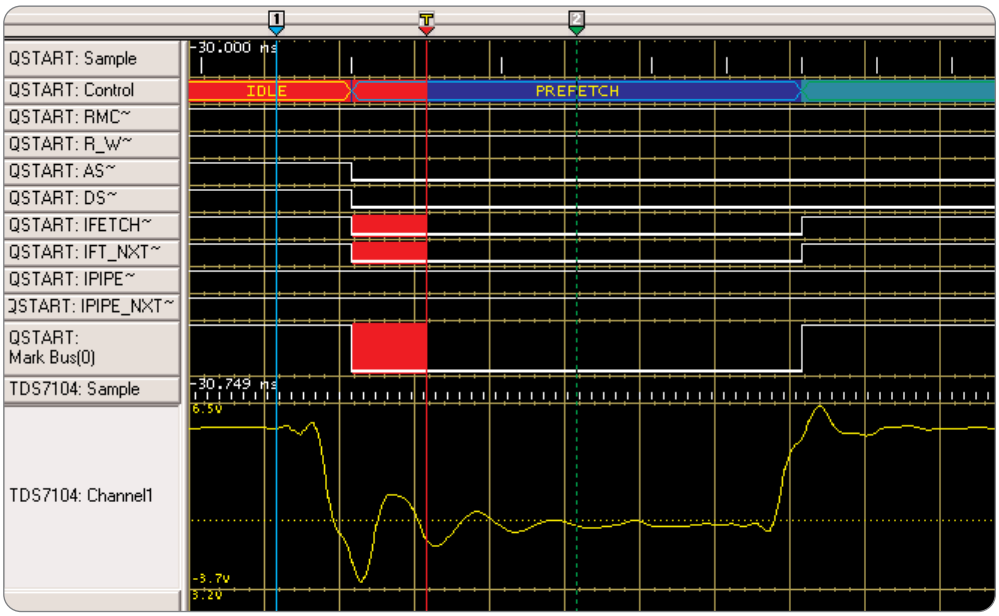


▶ ***Figure 2.*** *Fast edge transition effects adjacent signal path.*

Reflections, crosstalk and ground bounce are a few of the issues that can occur in the signal paths of digital circuit boards when the designer hasn't considered the effects of board runs and terminations on high-speed signal transitions. Circuit board signal paths designed for lower speed signals can become transmission lines when carrying higher frequency signals.

Reflections occur when signal energy, in improperly terminated circuit board runs, reflects from the receiving device back down the signal path to the sending device. Figure 1 shows the result of a reflection as a slight step in the rising edge of the waveform. The negative edge of the reflection goes below the threshold voltage and then transitions high appearing as a second transition. Notice that the logic analyzer detected this as a glitch as shown by the red flag in the LA 1: Glitch waveform. The higher resolution of LA 1: Mag_Glitch (500 ps) actually displays the glitch. Depending on the hold time of the input data, the output may change to an erroneous state. Reflections occurring on the data input can cause the output of the device to be unstable.

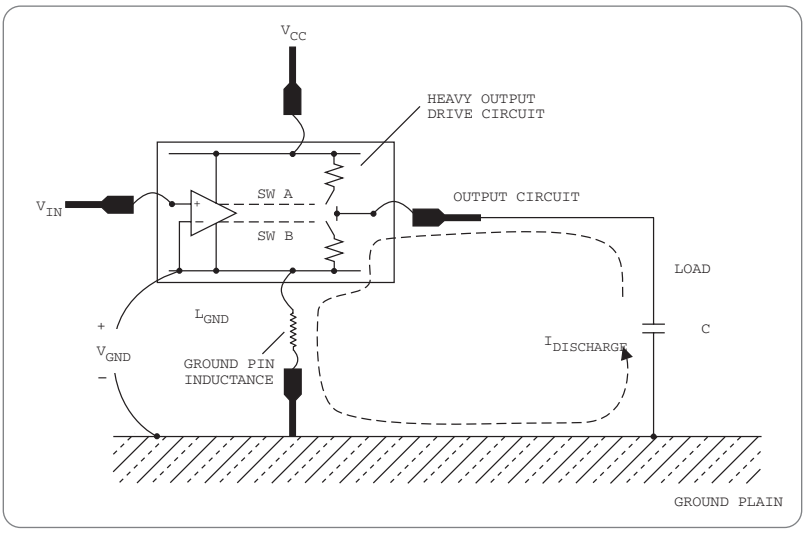
Crosstalk occurs when a fast transitioning signal in one circuit board run is coupled (capacitively and inductively) to an adjacent signal path. In Figure 2, the transition shown in the TDS7104: Channel2 waveform induces crosstalk into the adjacent signal path



▶ ***Figure 3.*** *Two analog traces showing the effects of ground bounce and the associated digital signal transitions.*

shown in TDS7104: Channel1 waveform. This glitch is displayed in the upper two digital waveforms. The LA 1: Chan 1(0) waveform, captured with 10 ns resolution, flags the occurrence of the glitch. The LA 1: Mag_Chan 1(0) waveform acquired at 500 ps intervals is able to display the glitch. When the crosstalk is sufficient enough, it causes the signal in the adjacent run to cross the threshold voltage which changes its logic state. If the crosstalk occurs during a clock transition, incorrect data will be loaded into the device. As with reflections, crosstalk is more likely to be a problem in circuit boards originally designed for lower frequency signals that are used in high frequency designs. High frequency design considerations are essential in reducing the effects of crosstalk.

Ground bounce is a shift in the device's ground reference caused by a current spike in the local ground plane. Figure 3 shows a low going transition (Channel 1) causing a narrow pulse to occur in the ground plane (Channel 2) as shown. One cause of ground bounce is the inductive voltage drop due to the current that flows through the ground when many signals transition simultaneously.



▶ ***Figure 4.*** *Current flow in the emitter causes voltage drop across the lead inductance.*

Figure 4 illustrates the voltage drop (V_{GND}) across the ground pin inductance caused by $I_{discharge}$ when the output level changes from hi to low. This shift in the ground reference essentially changes the threshold voltage at the input of the device. The device will not detect valid data due to the temporarily skewed threshold voltage reference. Ground bounce, when it occurs on a clock signal, may appear as a second clock pulse and can cause the device to clock erroneous data.

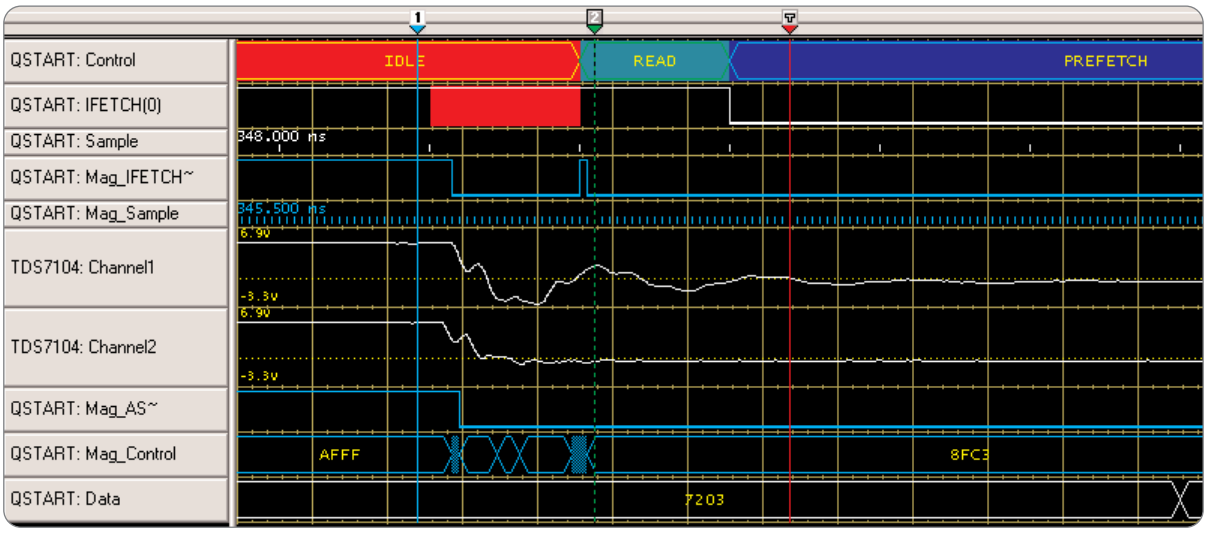
Step #3 - The Solution

Any of the above analog characteristics, occurring on a digital signal, can cause a system to malfunction. You can view these anomalies on an analog oscilloscope display, but how do you know that the analog signal you are viewing corresponds to the digital event that caused the problem? The answer seems simple — simultaneously look at correlated waveforms of the digital and the analog signals on an integrated display.

In the past, viewing both digital and analog signals with high accuracy timing resolution was primarily done using a logic analyzer and an oscilloscope. The designer could view both signals but they were on different displays that were not time correlated. Accurately relating the digital symptom to the analog cause was difficult and time consuming.

This method of debugging timing related system failures has been used because there wasn't a better way to view both digital and analog signals. (Note: Some logic analyzers have internal Digital Storage Oscilloscope (DSO) capability. However, internal DSO modules generally do not have the measurement performance of a stand-alone oscilloscope.)

Tektronix Integrated View (iView) integrates the operation of all Tektronix Logic Analyzers (TLA) with various models of Tektronix Digitizing Oscilloscopes (TDS). The "SETUP" and "RUN" functions of both instruments are done from the logic analyzer display.



▶ ***Figure 5.*** *Digital and Analog Time Aligned Signals on One Display.*

Using the iView software Setup Wizard, the TLA application automatically sets up the logic analyzer and oscilloscope cross-triggering, captures and displays both the analog and digital data, time-correlated, on one integrated display. Figure 5 shows the result of using iView software. Both the digital and the analog waveforms of the same signals are shown on the TLA display. The sample speed and measurement accuracy of a Tektronix Oscilloscope is fully integrated with the multi-channel and powerful triggering capabilities of a Tektronix Logic Analyzer.

Step #4 - The Applications

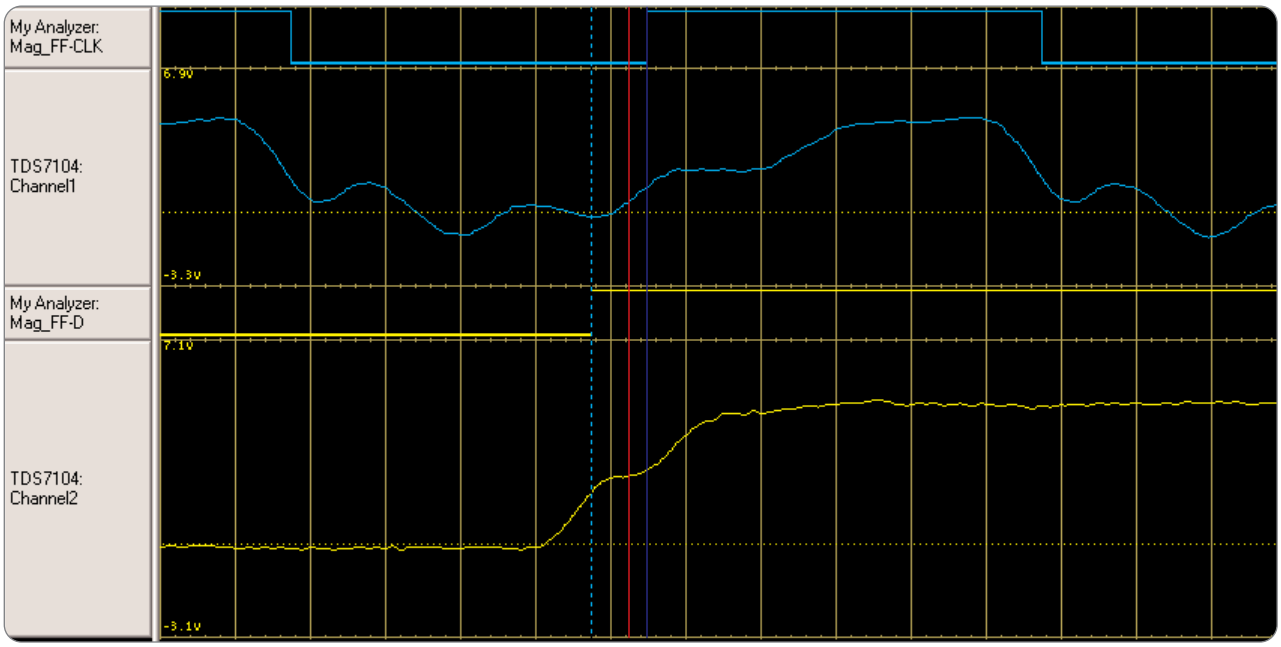
How does integrating a logic analyzer and an oscilloscope simplify and speed up the debug process of your design? If you are primarily concerned with viewing the analog characteristics of signals, what capability does a logic analyzer have that will help you?

While the oscilloscope has powerful analog measurement capabilities, typically, it is only able to look at four signals simultaneously and its triggering capability is generally intended to look for analog phenomena. However, the logic analyzer is able to monitor up to thousands of digital signals simultaneously and to trigger on a wide range of logic conditions.

The logic analyzer first “finds” a digital problem, such as a setup and hold violation, a glitch, or incorrect bus data, and then triggers both the logic analyzer and the oscilloscope. The oscilloscope acquires the analog characteristics of the “digital” signal. On some models, the oscilloscope’s trigger can also be selected to trigger the logic analyzer. Triggering on analog symptoms is also helpful in debugging systems.

The strengths of the best logic analyzer and the highest performance and most accurate oscilloscope are combined into one display to enable you to quickly verify and debug your design. The logic analyzer points to the problem and the oscilloscope looks at the problem with very high-resolution analog detail.

The following application examples show how being able to view time correlated digital and analog signals on the same display make it easier and more expedient to debug your system.



▶ ***Figure 6.*** *Digital and Analog Display of Setup/Hold Violation.*

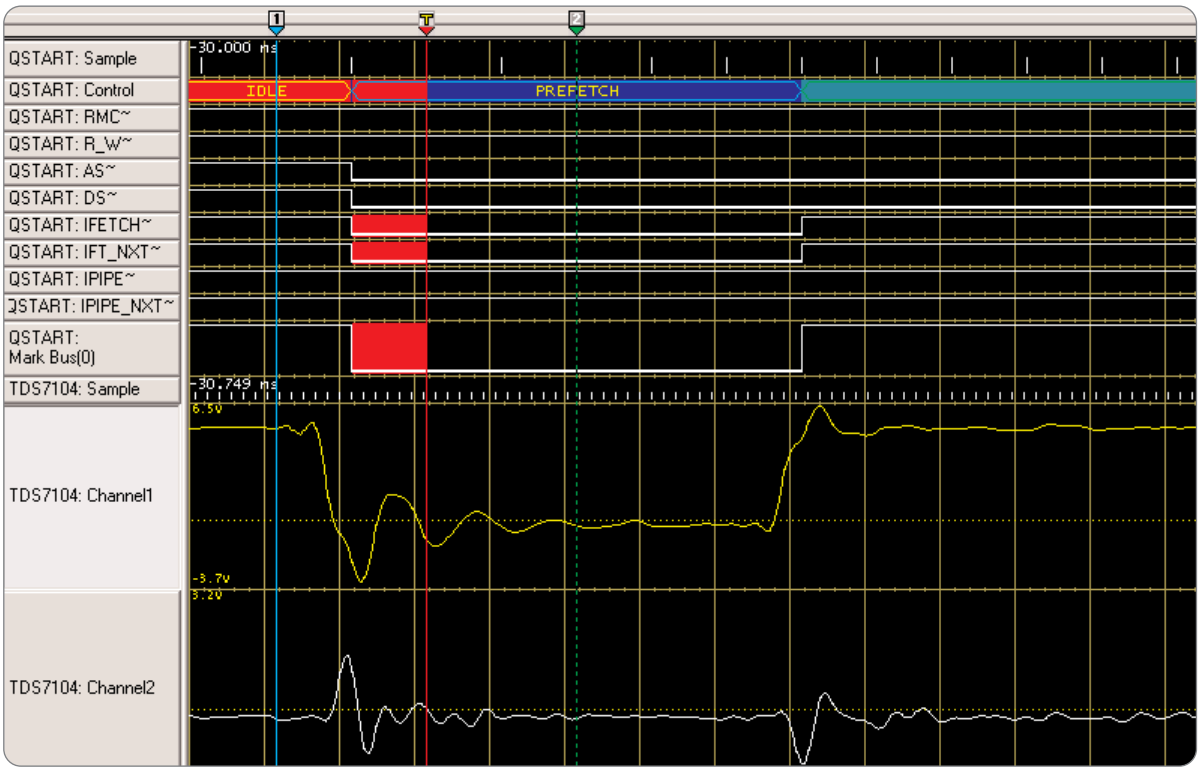
Application #1 Triggering on and Analyzing Setup/Hold violations

As digital systems speed increased, the amount of time for the data to stabilize prior to the clock has decreased significantly. Digital device manufacturers specify the time that the input signal must be stable before (setup) and after (hold) the clock edge to assure that the data will be correctly latched to the output. When the signal transitions inside the setup/hold window, a setup/hold violation occurs which can cause the system to fail. Crosstalk and reflections on clock and data signals can contribute to the degradation of the signal causing setup/hold violations. With the digital signals and the corresponding analog signals viewable on the same display, precise timing measurements of setup and hold violations are possible.

Figure 6 shows the logic analyzer triggering on a setup violation and the corresponding analog clock and data signals.

The LA triggered because the 2.5 ns setup time specification for the input data was violated. The lower two traces show the Clock signal (Channel 1) and the D-Input (Channel 2). The high timing resolution of the analog oscilloscope shows that the negative edge slew rate of the input signal is too slow and does not cross the threshold before the 2.5 ns setup time required for this device.

iView software simplifies the task of determining the cause of the problem by time-aligning the digital data with that of a high performance analog oscilloscope.



▶ ***Figure 7.*** *Data bus signals transition causing a shift in the ground voltage level.*

Application #2 Triggering on and Analyzing Ground Bounce Problems

Fast transitioning edges of bus signals, especially from high to low levels, can cause current spikes in the ground plane of a device.

Figure 7 shows the ground bounce (TDS7104: Channel2 waveform) caused by the digital bus signals (upper traces) transitioning low. The clock signal (TDS7104: Channnel1 waveform) has ringing on the trailing edge as a result of the ground bounce. The clock signal shows a short pulse following the negative clock edge. This unwanted signal, known as a glitch, crosses the voltage threshold causing erroneous data to be clocked into the device. The solid bars in the digital signals indicate that the logic analyzer triggered on and stored this glitch. The glitch occurred during the time just prior to the Trigger (vertical solid line after the solid bars). The logic analyzer, with iView software, also triggered the oscilloscope. The oscilloscope captured the analog characteristics of the clock signal. Note, that while the trigger point shown in Figure 7 is not that of the oscilloscope, the digital and the analog data are time aligned so the analog characteristics of the digital glitch, which triggered the logic analyzer, are being displayed.

Summary

iView software integrates the operation of designated Tektronix TDS Series Oscilloscopes with all TLA Series logic analyzers, and displays time-correlated views of both digital and analog waveforms on the same logic analyzer display. Designers need to view fast analog waveform details and correlate them on the logic analyzer display with the equivalent digital events to solve signal integrity challenges.

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